Wafer-Scale Epitaxial Graphene and Graphene Nanoribbon Arrays on SiC

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Graphene's properties make it attractive for high-speed electronic applications. When SiC is annealed at high temperatures, its top layers can decompose leading to loss of Si, while the remaining C atoms form epitaxial graphene layers on the SiC surface (subtractive epitaxy). Growth of graphene on the Si-face of hexagonal SiC wafers, 4H- or 6H-(0001) polytypes, exhibits manageable growth kinetics – contrary to the C-face – allowing good control over the number of graphene layers. Furthermore, the azimuthal orientation of epi-graphene on the Si-face of the SiC wafer is constant as it is determined by the single crystal substrate. Thus, there is a viable pathway towards graphene with uniform coverage and structural coherence at wafer-scale. By combining surface preparation steps in disilane/He with a higher temperature graphenization step in Ar and optimizing the process parameters for graphene growth on 4H(0001) SiC with 0.00° miscut, we have measured average Hall mobilities μ up to 4900 $cm^2\ V^{-1}\ s^{-1}$ at sheet carrier densities $N\sim4x10^{11}\ cm^{-2}$, after a long exposure to ambient atmosphere. We explain this large improvement in mobility by taking into account several factors, including the static gating effect imposed by the attachment of negative ions (e.g. OH) on the graphene surface after device fabrication, Coulomb and short-range scattering mechanisms, and evidence of scatterer transparency in the low carrier density, long-wavelength regime, where an abrupt increase in mobility is observed.[1] A plot of μ vs. N will be introduced as a benchmark of epi-graphene quality, and the effect on μ of the Hall bar size and orientation relative to the vicinal steps will be described. The epi-graphene produced with the above-described methods has been used in the fabrication of graphene integrated circuits and high performance RF transistors. Graphene grown on pit-free H_2-etched SiC (0001) surfaces will also be described, as will be the structure and interlayer twist angle trends of few layer graphene films grown on the C-face of SiC $(000\ \bar{1})$. Finally, a multistep process for fabricating arrays of the narrowest parallel epitaxial graphene nanoribbons (GNR) demonstrated to date will be described. This is a hybrid process using the self-assembly properties of a lamella-forming block copolymer (BCP) to create parallel GNR arrays bounded by pairs of parallel lines fabricated topdown by e-beam lithography on graphene grown epitaxially on SiC wafers.[2] The carrier confinement due to the GNR patterning is expected to open a band gap in the electronic energy spectrum of 2D graphene.

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1. D. B. Farmer, V. Perebeinos, Y.-M. Lin, C. Dimitrakopoulos, Ph. Avouris ***Phys. Rev. B.* 84**, 205417 (2011).
2. G. Liu, Y. Wu, Y.M. Lin, D. Farmer, J. A. Ott, J. Bruley, A. Grill, Ph. Avouris, D. Pfeiffer, A. A. Balandin, C. Dimitrakopoulos ***ACS Nano* 6**, 6786–6792 (2012).

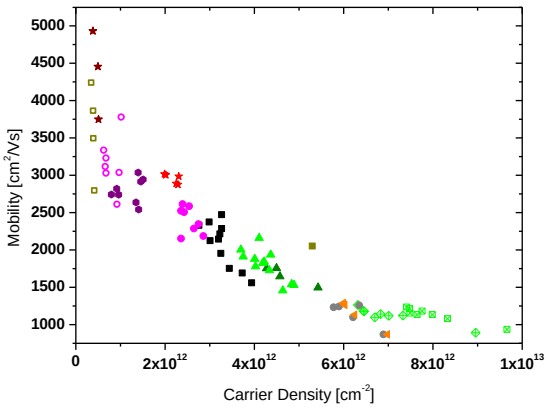

Figure 1: Plot of μ vs. N for devices built on many graphene samples grown with the optimized *beta* tool process (all points except khaki squares). The benchmark of graphene quality is defined to be a plot of μ vs. N.

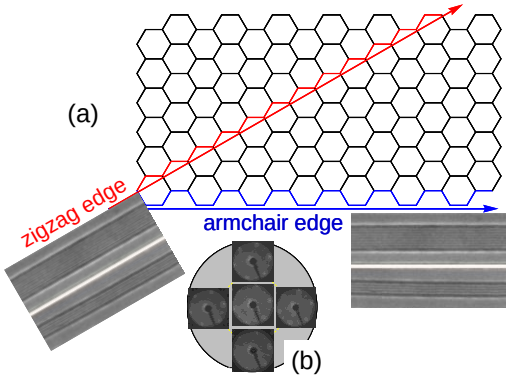

Figure 2: Knowing the constant azimuthal orientation of epi-graphene on SiC (0001) allows to chose the general orientation of GNR arrays fabricated using our hybrid method comprising BCP self assembly and e-beam lithography[2]