Graphene crystal growth and device integration

Luigi Colombo, Robert M. Wallace and Rodney S. Ruoff
Texas Instruments Incorporated, Dallas, TX 75243
University of Texas at Dallas, Richardson, TX 75080
University of Texas at Austin, Austin, TX 78712
colombo@ti.com

In the past decade, the state of the art Si-based electronics has scaled devices from about 100 nm to the about 20 nm with a defined pathway to devices, logic and memory, of about 15 nm. Graphene has been the subject of considerable theoretical and experimental interest because of its unique transport properties together with exceptional chemical and physical properties. New devices taking advantage of the theoretical prediction on the existence of a Bose-Einstein condensate (BEC) in bi-layer graphene films have been proposed. Yet others have been proposed that take advantage of the properties of bilayer graphene modifications of graphene to achieve a finite bandgap. In order to demonstrate the existence of a BEC or any other graphene devices, high quality films will have to be developed and integrated with dielectrics and metal contacts. High quality graphene can be formed by exfoliation from natural graphite with sizes of a few hundred square microns. The recent discovery of growth of large-area and monolayer graphene growth on Cu substrates has opened many opportunities for the development of graphene-based devices. In order to take full advantage of the fundamental properties of graphene and the synthesis of large area films it is necessary to grow uniform and nearly defect-free films as the semiconductor industry has done with silicon substrates. In this presentation I will review the growth of large area graphene and integration of dielectrics and metals with graphene and their effects on field effect transistors characteristics.